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EXAMINER	
TRUJILLO, JAMES K	

ART UNIT	PAPER NUMBER
2116	7

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/749,088	Applicant(s) ADACHI, MITSUHIRO	
	Examiner James K. Trujillo	Art Unit 2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☒ Claim(s) *20 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The office acknowledges the receipt of the following and placed of record in the file: Declaration dated 2/26/01, Drawings dated 4/30/01, CFR dated 5/21/01, and CFR dated 8/13/01.

2. Claims 1-21 are presented for examination.

Claim Objections

3. Claims 15-17 are objected to because of the following informalities: all references to "the circuitry" should be changed "circuitry". Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 15-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 15-17 recites the limitation "the circuitry" in line 2 of each of the respective claims. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-9 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomas et al., U.S. Patent 6,216,235 in view of Casal et al., U.S. Patent 5,822,596.

9. As to claim 1, Thomas taught a method comprising:

a. determining if a predetermined limit of global functional activity (temperature due to activity) in an integrated circuit has been met or exceeded (temperature has become dangerously high) [col. 3 lines 21-30];

b. and if so, then:

i. reducing a high frequency (FMAX) of clocking of circuitry gradually to zero (the minimum frequency may be zero) to stop the clocking of circuitry [col. 3 line 52 through col. 4 line 22 and figure 2];

Thomas teaches detecting the temperature as a global functional activity. Thomas then teaches that if the temperature is met or exceeded the frequency of operation of clocking circuitry is then gradually reduced (including if necessary to a zero frequency).

Thomas does not expressly disclose waiting a predetermined time after stopping the clocking of circuitry and starting the clocking circuitry at a low frequency.

Casal teaches waiting a predetermine time (sufficient stabilization time) after stopping (powering down) the clocking of circuitry (for logic ciruits) and starting the clocking circuitry at a low frequency [col. 1 line 56-61, col. 1 line 56 through col. 1 line 4 and col. 3 line 58 through col. 4 line 11].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Thomas by waiting a predetermined time after stopping the clock and starting the clocking circuitry at a low frequency as taught by Casal. Thomas and Casal are both directed toward controlling clocks of a computer system. An artisan would have been motivated because Casal teaches that waiting for predetermined times between changing clock frequency and starting clocking circuitry at a low frequency avoids transients that are harmful in electronic components [col. 1 lines 16-21 and col. 1 lines 56-61]. Avoiding transients is desirable in computer systems such as Thomas.

10. As to claim 2, Thomas together with Casal taught the method according to claim 1 described above. Thomas further taught wherein if the determining if the predetermined limit of global functional activity in the integrated circuit has not been met or exceeded, it is repeated [col. 3 lines 38-lines 67]. Thomas discloses using a temperature sensor to determine if the limit has been met or exceeded. In doing so, Thomas clearly must continually determine the temperature. In Thomas, the determining step must be repeated to determine a change in temperature.

11. As to claim 3, Thomas together with Casal taught the method according to claim 1 described above. Thomas and Casal do not expressly disclose wherein the predetermined time is a number of clock cycles of a free-running clock of the integrated circuit. However, both Thomas and Casal each use a free-running clock. Casal teaches at col. 4 lines 1-11 that an appropriate amount of time is required at each frequency of operation. One of ordinary skill in the art would have recognized that a free-running clock is used to measure time by counting its clock cycles. It would have been obvious to one of ordinary skill at the time of the invention to

use the free-running clock to determine the predetermined time using a number of clock cycles of the free running clock of the integrated circuit because the free-running clock is an available mean to determine time and is readily available in the existing circuitry.

12. As to claim 4, Thomas together with Casal taught the method according to claim 1 described above. Thomas further taught at col. 12, lines 3-7, and Casal taught at col. 1, lines 56-61, the reducing of the high frequency clocking of circuitry gradually to zero incluces:

a. clocking the circuitry at a first frequency; and

b. before clocking the circuitry at a second frequency lower than the first frequency, waiting a predetermined time during the clocking of the circuitry at the first frequency.

Specifically, Thomas discloses "... a controllable frequency of the clock is gradually and *successively stepwise reduced* as needed to regulate thermal conditions." Successively stepwise reduced clearly implies, or at the very least an artisan would recognize that it implies, that in reducing the clock frequency the clock is reduced to lower frequencies only after waiting a predetermined time at a particular frequency.

Casal discloses that a clear need, which his invention satisfies, is a "...system and method for accomplishing a *step-by-step increase and* ***decrease*** *of a clock frequency*... such that a *sufficient number of steps and sufficient stabilization time* at each step is provided..." Step-by-step increase and decrease with sufficient stabilization time clearly teaches changing frequencies from a first frequency to a lower second frequency only after waiting a predetermined time.

13. As to claim 5, Thomas together with Casal taught the method according to claim 1, described above. Casal further taught at col. 1, lines 56-61, wherein after starting the clocking of the circuitry at the low frequency, the method further includes gradually increasing the frequency

of the clocking of the circuitry to the high frequency. Specifically, Casal taught that the step-by-step change in the clock frequency would also be applied during a startup of the system.

14. As to claim 6, Thomas together with Casal taught the method according to claim 5 described above. As set forth hereinabove for the same reasons, Casal also teaches the gradual increasing of the frequency of circuitry to the high frequency includes clocking circuitry at a first frequency, and before clocking the circuitry at a second frequency higher than the first frequency, waiting a predetermined time during clocking of the circuitry at the first frequency. Specifically, Casal teaches that the step-by-step increase would be applied at startup.

15. As to claim 7, Thomas together with Casal taught the method according to claim 1 described above. Thomas further taught at col. 7, lines 13-34, wherein the global functional activity (temperature due to activity) in the integrated circuit is proportional to temperature of the integrated circuit (microprocessor) and the predetermined limit (temperature is determined to be "hot") of global functional activity is proportional to an expected temperature of the integrated circuit. Thomas discloses using a temperature sensor that is integrated with a microprocessor circuit. The sensor is used to determine the temperature due to processing activity.

16. As to claim 8, Thomas together with Casal taught the method according to claim 1, described above. Thomas inherently teaches wherein the reducing of the high frequency clocking of the circuitry gradually to zero avoids large variations in the current associated with a rapid shut-off of the clocking of circuitry. Thomas gradually reduces the clock frequency that must avoid large variations in the current as those associated with a rapid shut-off of the clocking circuitry. Casal also teaches at col. 1, lines16-21 and col. 1, line 56 through col. 1, line 4,

gradually decreasing a high frequency to zero using a step-by-step decrease thereby avoiding current transients during a shutdown.

17. As to claim 9, Thomas together with Casal taught the method according to claim 5 described above. Casal further taught at col. 1, lines16-21 and col. 1, line 56 through col. 1, line 4 the starting (when powering up) of the clocking of the circuitry at the low frequency and the gradual increase in the frequency of the clocking of the circuitry to the high frequency avoids large variations in current (current surge) otherwise associated with a rapid turn-on of the clocking of circuitry.

18. Claims 10-12, 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomas.

19. As to claim 10, Thomas teaches a circuit comprising:

a. a clock generator (oscillator 8, 22, 52 and clock input of different embodiments) to generate a clock [figures 1, 3, 4, 5, 9 and 10];

b. an activity detector (activity detector) to measure global functional activity of the circuit and temperature sensor (temperature due to processor activity) [figures 3, 5, 7, 9, and 10; col. 4 lines 30 et seq.];

c. a clock throttling controller (clock regulation unit 20) coupled to the activity detector and the clock generator, the clock throttling controller to generate a throttled clock to couple to functional blocks (i/o ports, instruction cache, current instruction, program counter) of the circuit for clocking circuitry therein, the clock throttling controller to gradually throttle the frequency of the throttled clock to the functional blocks in response

to the measure of the global functional activity meeting (reaching a lower) or exceeding (falling below a lower limit) a predetermined limit [col. 5 line 38 through col. 6 line 9].

Thomas also teaches the case wherein the temperature causes the clock to be throttled in response to activity. If the activity were very high for a sustained period of time the temperature would reach above a predetermined threshold causing throttling to take place [col. 4 lines 1-22].

Thomas does not expressly disclose wherein the clock generator, activity detector and clock throttling controller are on an integrated circuit. Official Notice is taken of the motivation and modification necessary to integrate devices on an integrated circuit, this is notoriously well known. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Thomas by manufacturing the clock generator, the activity detector and the clock throttling circuit on the same integrated circuit because integrated circuits often have a plurality of different devices. One of ordinary skill in the art would have made the modification because one of ordinary skill would have recognized that doing so would reduce cost, increase speed and increase reliability all of which would be highly desirable in Thomas.

20. As to claim 11, Thomas as set forth hereinabove, taught the integrated circuit as according to claim 10. Thomas further taught, at col. 4 lines 30-35, wherein the activity detector receives measures of local functional activity associated with each functional block of the integrated circuit to measure the global functional activity of the integrated circuit. Wherein interrupt controllers, input/output ports, instruction cache, current instruction, and program counter are interpreted to be functional blocks of the integrated circuit. Thomas uses the activity

of different functional blocks to make a determination as to the global activity of the microprocessor.

21. As to claim 12, Thomas, as set forth hereinabove taught the integrated circuit according to claim 10. Thomas further teaches at, col. 4 lines 30-35, the activity detector receives measures of local functional activity associated with each functional block of the integrated circuit to determine the measure of the global functional activity of the integrated circuit, as set forth hereinabove. Thomas further teaches at, col. 4 lines 30-45, the activity detector compares the measure of the global functional activity with the predetermined limit to determine if it is met or exceeded (if processing is needed or not). Thomas monitors functional blocks of the microprocessor to determine the global processing of the microprocessor. Thomas also teaches at, col. 4 lines 30-45, the activity detector signals to the clock-throttling controller (if processing is needed the VCO controller is notified) whether or not the predetermined limit has been met.

22. As to claim 13, Thomas, as described above, taught the integrated circuit according to claim 10. Thomas does not expressly disclose the limitations of claim 13. In summary, Thomas teaches gradually throttling the clock using a control signal based on activity to control the frequency of an oscillator [figure 3].

Casal taught a logical gate (CLK input at 208) coupled to a clock generator to receive the clock and the clock throttling controller (divider 104) to receive a control signal (227), the logical gate to periodically mask out one or more clock cycles of the clock (at 110) to generate the throttled clock in response to the control signal to gradually throttle the frequency of the throttled clock [figures 2, 4, 5, col. 1 line 65 through col. 2 line 14 and col. 4 line 51 through col. 7 line 29]. Casal gradually reduces the clock during to avoid transients. Casal reduces the clock

by decreasing the frequency in a gradually manner using frequency dividers. Casal uses a clocked RS flip-flop (208) that periodically masks out one or more clock cycles.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Thomas by substituting the VCO and VCO controller of Thomas with the clock system and frequency controlling circuitry of Casal. Both inventions are directed toward controlling a clock. An artisan would have made the modification because Casal teaches that his invention desirably reduces transients, which are harmful to electronic circuits [col. 1 lines16-21]. One of ordinary skill would have recognized that reducing transients is desirable in Thomas.

23. As to claim 14, Thomas together with Casal taught the method according to claim 14 described above. Casal further taught wherein the logical gate is and AND gate to logically AND the clock and the control signal from the clock throttling controller together. Specifically, Casal discloses wherein the control signal and the clock signal are coupled to a clocked RS Flip-Flop (FF). The control signal is coupled to the S input of the RS FF. The clock signal is coupled to the Clock input of the RS FF. It is well known and inherent in the art that the S input and the Clock input are logically ANDed.

24. As to claim 15, Thomas taught the integrated circuit according claim 10, described above. Thomas does not expressly disclose wherein one hundred percent of circuitry in the functional blocks can have the throttled clock stopped. Thomas discloses that the clocks can be set to a sleep clock that near the minimum frequency fMIN [col. 4 lines 58-59]. Thomas also discloses wherein fMIN may be zero [col. 4 lines 5-7].

Official Notice is taken of systems with sleep clocks wherein the sleep clock has a zero frequency. It would have been obvious to one of ordinary skill in the art at the time of the

invention to modify Thomas by reducing the sleep clocks to zero frequency to further reduce power consumption as desired by Thomas.

25. As to claim 16, Thomas taught the circuit according to claim 10 described above. Thomas further taught wherein less than one hundred percent of the circuitry in the functional blocks can have the throttled clock stopped [col. 4 lines 5-8]. Thomas teaches that there are some types of circuitry within a functional block (memory) that may require some minimum nonzero frequency.

26. As to claim 17, Thomas taught the circuit according to claim 16, described above. Thomas further taught only the circuitry to which the throttled clock can be stopped is the throttled clock coupled and its frequency gradually throttled in response to the measure of functional activity meeting or exceeding the predetermined limit [col. 4 lines 5-8].

27. As to claim 18, Thomas taught the integrated circuit according to claim 10 described above. Thomas further taught wherein, the frequency of the throttled clock is gradually throttled in response to the measure of the functional activity meeting or exceeding the predetermined limit [col. 4 lines 46-64]. In summary, Thomas gradually throttles down a clock when activity is below a certain predetermined level. Thomas gradually throttles up a clock when activity is above a certain predetermined level.

Thomas does not expressly throttle *OFF* and the *ON* in response to the measure of activity. Official Notice is taken of systems with sleep clocks wherein the sleep clock has a zero frequency. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Thomas by throttling the sleep clocks to zero frequency to further reduce power consumption as desired by Thomas. An artisan would recognize that having a

environment where the clocks are reduce to zero that the clock must also be throttled on when activity reaches the predetermined level resulting in the claimed invention.

28. As to claim 19, Thomas taught the claimed integrated circuit therefore he also taught the claimed clock generator.

Allowable Subject Matter

29. Claims 20 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

30. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat. No. 5,956,653 to Kink et al. This patent teaches reducing thermal stresses by having a controlled power on.

U.S. Pat. No. 5,490,059 to Mahalingaiah. This patent teaches adjusting the clock speed gradually and incrementally based on temperature.

U.S. Pat. No. 6,397,343 to Williams et al. This patent teaches adjusting the clock frequency in a graphics subsystem.

U.S. Pat. No. 5,768,213 to Jung et al. This patent teaches turning off a clock for a particular unused function block.

U.S. Pat. No. 6,158,012 to Watts, Jr. This patent teaches adjusting the system clock based on activity and temperature.

U.S. Pat. No. 5,996,083 to Gupta et al. This patent teaches supplying a clock to a particular functional unit based on a power control register.

Japan Pat. No. 405011877 A to Fujimura. This patent teaches starting a computer after reset with a low frequency.

Marculescu, D.; "Profile-driven code execution for low power dissipation", Low Power Electronics and Design, 2000. ISLPED '00. Proceedings of the 2000 International Symposium on, 26-27 July 2000, Pages: 253 – 255. This paper teaches a method for power-performance trade-off.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (703) 308-6291. The examiner can normally be reached on M-F (7:30 am - 5:00 pm) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703) 305-9717. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

James Trujillo
January 22, 2004

THOMAS LEE
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